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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/751,813
Filing Date: December 29, 2000
Appellant(s): SPRUNT ET AL.

Ashley R. Ott
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on September 22, 2006 appealing from the Office action mailed on March 17, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,835,705	LARSEN et al.	9-1998
6,205,468	DIEPSTRATEN et al.	3-2001
5,657,253	DREYER et al.	8-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,705 to Larsen et al. ("Larsen") in view of U.S. Patent No. 6,205,468 to Diepstraten et al. ("Diepstraten") in view of U.S. Patent No. 5,657,253 to Dreyer et al. ("Dreyer").

The above ground(s) of rejection were set forth in the final Office action mailed on March 17, 2006 and are reproduced at page 11 of this examiner's answer for completeness.

(10) Response to Argument

Appellant contends generally that Larsen does not disclose or suggest a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of a class of events in order to select an event that belongs to a subclass that is not masked (brief, page 10, last paragraph), and similarly that Diepstraten does not disclose or suggest this feature (brief, page 11, first paragraph).

However, as noted in the final Office action and again in the advisory action mailed on June 7, 2006, it is a combination of references that teaches or suggests this feature. One cannot

show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981), and *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Larsen discloses the event selection control register (ESCR) and the first multiplexer as recited in the claim (see, for example, control registers 80 and multiplexer 82 in FIG. 2). Larsen further discloses selecting an event that is not masked based on control signals from the ESCR (see, for example, column 5, lines 9-17). It is noted that Appellant does not present any arguments contrary to this interpretation. Larsen does not expressly disclose a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

Diepstraten, however, discloses an event masker coupled to a control register to mask, based on control signals from the control register, ones of the events in order to yield at least some of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-45). Diepstraten further discloses that the event masker reduces the number of events that the apparatus must process (column 4, lines 45-47). In other words, the event masker "filters out" extraneous events. Thus, in view of Diepstraten's teachings, it would have been obvious to a person having ordinary skill in the art to incorporate an event masker into Larsen, so as to reduce the number of events that Larsen's apparatus must process.

Diepstraten does not expressly disclose that the event masker is implemented in the form of "a second multiplexer." Nonetheless, Diepstraten states, "Those skilled in the art may perceive other ways to effect selectivity that are, nonetheless, within the broad scope of the

present invention" (column 4, lines 48-50). Indeed, Larsen teaches one such way to effect selectivity. Specifically, Larsen discloses a means for selecting events that is implemented in the form of one or more multiplexers (see, for example, multiplexer 82a and multiplexer 82b in FIG. 3, and column 5, lines 30-36). Thus, in view of Larsen's suggestion, it would have been obvious to a person having ordinary skill in the art to similarly implement a means for masking events, such as Diepstraten's event masker, in the form of a multiplexer.

Therefore, the combined teachings of the references would have suggested to those of ordinary skill in the art, a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of a class of events in order to select an event that belongs to a subclass that is not masked. The examiner respectfully submits that the record sets forth a *prima facie* case of obviousness.

Appellant more specifically contends that the structure of the event mask register 90 in Diepstraten is not the same as the structure of the recited second multiplexer because it is not connected to a first multiplexer and to an ESCR (brief, page 12, second paragraph), and that the functioning of the event mask register 90 is not the same as the functioning of the recited second multiplexer because it does not mask a class of events received from the first multiplexer based on control signals from the ESCR (brief, page 12, last paragraph).

However, it is respectfully submitted that Appellant mischaracterizes Diepstraten's event masker. As noted in the advisory action, the event mask register 90 is not in and of itself the event masker. Rather, Diepstraten indicates that the event mask register 90 is the control register for the event masker (see, for example, column 12, lines 36-57), and is thus analogous to the recited ESCR. While Appellant "can find no disclosure or suggestion in Diepstraten of a

separate 'event masker' unit controlled by the event mask register 90" (brief, page 12, second paragraph), Diepstraten illustrates such a unit in FIG. 10. Diepstraten illustrates that the event masker comprises, at minimum, AND gate 580, which is coupled to event flip-flop output 570 and to the event mask register 90 (see, for example, column 23, lines 37-47). The event mask bit 558 (FIG. 10) is a control signal from the event mask register 90.

Thus, the structure of Diepstraten's event masker is such that it is connected to a preceding event output and to a control register. The functionality of Diepstraten's event masker is such that it masks events received from the preceding event output based on signals from the control register (see, for example, column 4, lines 42-45, and column 23, lines 37-47).

Appellant further states that the event mask register 90 in Diepstraten is not a multiplexer at all, but is rather a register (brief, page 13, first paragraph).

The examiner agrees; the event mask register 90 is a register. However, as noted above, Diepstraten's event masker comprises AND gate 580. Diepstraten's event masker teaches or suggests the functionality of the recited second multiplexer in that it "masks ones of the events to yield the at least some of the events" (column 4, lines 42-45). The difference, of course, is that Diepstraten's event masker is not realized in the form of a multiplexer. However, Larsen in view of Diepstraten suggests such a multiplexer to a person having ordinary skill in the art.

Appellant further contends that the two multiplexers illustrated in FIG. 3 of Larsen operate in parallel on separate threads and do not operate in the same manner as the first and second multiplexers recited in the claim (brief, page 13, first paragraph).

However, the multiplexers of Larsen correspond to the recited first multiplexer. It is noted that the two multiplexers illustrated in FIG. 3 are also represented conceptually as multiplexer 82 in FIG. 2. The examiner does not imply that one of Larsen's multiplexers is to assume the role of the recited second multiplexer. Instead, it is Diepstraten's event masker that corresponds to the recited second multiplexer. As noted in the advisory action, Larson's disclosure of two multiplexers operating in parallel is not evidence that a multiplexer is somehow unsuitable as a means for masking events.

Moreover, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In Larsen's apparatus, the preceding event output from which Diepstraten's event masker would receive "a class of events" is the multiplexer 82. As noted above, the multiplexer 82 in Larsen corresponds to the recited first multiplexer. Larsen discloses classes of events in terms of "event groups" (see, for example, column 5, lines 41-43). One class of events includes IU/FX/FP events (see, for example, block 176 in FIG. 4), another class of events includes SC events (block 184), and another class of events includes BIU/LB/L2 events (block 192). Likewise, in Larsen's apparatus, the control registers 80 would supply "a second set of control signals" to the event masker in a manner comparable to that of Diepstraten's event mask register 90. As noted above, the control registers 80 in Larsen correspond to the recited event selection control register (ESCR). Larsen discloses that the control registers 80 include several bit fields (see, for example, column 5, lines 13-17). It would have been within the level of ordinary skill

in the art to extend the control registers 80 as necessary to include a bit field for event mask bits, such as the event mask bit 558 in Diepstraten.

Appellant contends generally that Dreyer does not disclose or suggest the recited second multiplexer, but as Appellant further notes, the final Office action does not rely on Dreyer for this feature (brief, page 13, second paragraph).

Appellant contends that because none of Larsen, Diepstraten or Dreyer individually disclose or suggest a second multiplexer coupled to an ESCR and a first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked, any combination of Larsen, Diepstraten and Dreyer does not disclose or suggest this feature (brief, page 13, last paragraph).

However, as noted in the advisory action, such a statement is not a persuasive argument against an obviousness rejection under 35 U.S.C. 103(a). In response, Appellant proposes that if none of the prior art references Larsen, Diepstraten and Dreyer discloses a particular feature of a claim, then logically there is no possibility that the combination of references can disclose or suggest the feature (brief, page 14, first paragraph).

However, the validity of such reasoning aside, Appellant is respectfully reminded that the test for obviousness is not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

The following table illustrates, in summary, how Appellant's claim 1 is mapped to the teachings of the references, with the "second multiplexer" feature highlighted:

1. An apparatus, comprising:	
a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;	**Larsen** (processor 10 in FIG. 1; multithreaded at col. 3, lines 39-55; events at col. 6, lines 58-61)
an event selection control register (ESCR) coupled to the processor;	**Larsen** (control registers 80 in FIG. 2)
a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor;	**Larsen** (multiplexer 82 in FIG. 2; event selection at col. 5, lines 9-17 and 41-43)
a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;	**Larsen** and **Diepstraten** (event mask register 90 in FIG. 3; AND gate 580 and event mask bit 558 in FIG. 10; event masking at col. 4, lines 42-50)
a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred; and	**Larsen** (FIG. 3 and col. 6, lines 10-23; qualify by thread ID at col. 6, line 54 to col. 7, line 3) and **Dreyer** (logic block 23 in FIG. 1; qualify by thread CPL at col. 4, lines 39-46)
an event counter to count the event qualified by the logic circuit.	**Larsen** (performance monitor counters 84 in FIG. 2)

Lastly, Appellant makes a final statement that the examiner "failed to search and find a printed publication or patent that discloses the claimed invention as set forth in MPEP § 706.02(a)" and thus "erred in rejecting claims 1, 3, 4, 7-9, 18, 20, 21, and 27-45 under [35] U.S.C. § 103(a)" (brief, page 15, last paragraph).

However, the examiner notes that MPEP § 706.02(a) discusses rejections under 35 U.S.C. 102(a), (b) and (e). No anticipation rejections under 35 U.S.C. 102(a), (b) or (e) were applied to the appealed claims. If Appellant is aware of such a printed publication or patent that the examiner inadvertently failed to find, it respectfully asked that Appellant provide the reference to the Office for consideration.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

* * *

The following ground(s) of rejection were set forth in the final Office action mailed on March 17, 2006 and are reproduced here for completeness:

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 4, 7-9, 18, 20, 21 and 27-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,705 to Larsen et al. (art of record, "Larsen") in view of U.S. Patent No. 6,205,468 to Diepstraten et al. (art of record, "Diepstraten") in view of U.S. Patent No. 5,657,253 to Dreyer et al. (art of record, "Dreyer").

With respect to claim 1 (currently amended), Larsen discloses an apparatus comprising:

(a) a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) an event selection control register (ECSR) (see, for example, control registers 80 in FIG. 2);

(c) a first multiplexer coupled to the ECSR to select a class of events, based on a first set of control signals from the ECSR, from a group of event signals issued from the processor (see, for example, multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows that the multiplexer selects events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor).

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(d) a second multiplexer coupled to the ECSR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker coupled to a control register for masking events based on control signals from the control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the apparatus of Larsen with the event masking features of Diepstraten, such that the apparatus comprises a second multiplexer coupled to the ECSR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(e) a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit coupled to the multiplexer, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer discloses a logic circuit coupled to an event selection control register and a multiplexer to qualify an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the apparatus of Larsen and Diepstraten with the thread CPL features of Dreyer, such that the apparatus comprises a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL). One of ordinary skill in the art would have been motivated to differentiate and qualify events based on

supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(f) an event counter to count the event qualified by the logic circuit (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events).

With respect to claim 3 (currently amended), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the ESCR comprises a first field of bits to store the first set of control signals to select the class of events (see, for example, Larsen, column 5, lines 9-17, which shows that the control registers have bit fields to store the control signals).

With respect to claim 4 (currently amended), the rejection of claim 3 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the ESCR further comprises a second field of bits to store the second set of control signals to mask the subclasses (see, for example, Diepstraten, event mask register 90 in FIG. 3, and see, for example, Larsen, column 5, lines 9-17, which shows that the control registers have bit fields to store the control signals).

With respect to claim 7 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the event counter is stopped and cleared before a new event is selected (see, for example, Larsen, column 4, lines 50-57, which shows software-writable event counters, and see, for example, Dreyer, column 3, lines 19-22, which shows resetting, i.e. stopping and clearing, the event counter with a software instruction).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter reset features of Dreyer, so as to stop and clear the counter values in software.

With respect to claim 8 (previously presented), the rejection of claim 7 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the event counter is preset to a certain state (see, for example, Larsen, column 4, lines 50-57, which shows software-writable event counters, and see, for example, Dreyer, column 3, lines 19-22, which shows presetting the event counter to a certain value or state).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the counter preset features of Dreyer, so as to enable functions such as countdowns (see, for example, Dreyer, column 4, lines 21-30).

With respect to claim 9 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the class of events includes hardware performance and breakpoint events (see, for example, Larsen, column 5, lines 47-56, which shows a class of events that includes hardware performance events such as instructions completed and processor cycles, and breakpoint events such as thread switch counts).

With respect to claim 18 (currently amended), Larsen discloses a method comprising:

(a) executing a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) instructing a first multiplexer, based on a first set of signals from an event selection control register (ECSR), to select a class of events from a group of event signals issued from the processor (see, for example, control registers 80 and multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows instructing the multiplexer to select events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor);

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(c) instructing a second multiplexer, based on a second set of signals from the ECSR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker for masking events based on control signals from a control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Larsen with the event masking features of Diepstraten, such that the method comprises instructing a second multiplexer, based on a second set of signals from the ECSR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(d) qualifying the event, by a logic circuit, based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread CPL.

However, Dreyer discloses a logic circuit for qualifying an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Larsen and Diepstraten with the thread CPL features of Dreyer, such that the method comprises qualifying the event, by a logic circuit, based on a thread ID and a thread CPL. One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(e) counting the event qualified by the logic circuit using an event counter (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events); and

(f) accessing the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 20 (previously presented), the rejection of claim 18 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the qualifying the event includes requiring that the event has a preselected thread ID (see, for example, Larsen, column 5, lines 27-30, which shows requiring that the event has a preselected thread ID such as "thread 0" or "thread 1").

With respect to claim 21 (previously presented), the rejection of claim 20 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the qualifying of the event further includes requiring that the event has a preselected thread CPL (see, for example, Dreyer,

column 4, lines 49-58, which shows requiring that the event has a preselected thread CPL).

With respect to claim 27 (previously presented), the rejection of claim 18 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 28 (previously presented), the rejection of claim 20 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred (see, for example, Larsen, column 6, line 54 to column 7, line 3, which shows that the thread ID represents the thread where the event occurred).

With respect to claim 29 (previously presented), the rejection of claim 21 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred (see, for example, Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 30 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred (see, for example, Dreyer, column 4, lines 39-46, which shows that the CPL indicates a current privilege level at which the thread is operating when an event is to be counted).

With respect to claim 31 (previously presented), the rejection of claim 1 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses an access location to allow access to the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 32 (currently amended), Larsen discloses a system comprising:

(a) a storage medium coupled with a processor (see, for example, main memory 52 and processor 10 in FIG. 1), the processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) an event selection control register (ESCR) coupled to the processor (see, for example, control registers 80 in FIG. 2);

(c) a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor (see, for example, multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows that the multiplexer selects events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor).

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(d) a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker coupled to a control register for masking events based on control signals from the control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen with the event masking features of Diepstraten, such that the system comprises a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(e) a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines

10-23, which shows a logic circuit coupled to the multiplexer, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread current privilege level (CPL).

However, Dreyer discloses a logic circuit coupled to an event selection control register and a multiplexer to qualify an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Larsen and Diepstraten with the thread CPL features of Dreyer, such that the system comprises a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID and a thread current privilege level (CPL). One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(f) an event counter to count the event qualified by the logic circuit (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events); and

(g) an access location to allow access to the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 33 (previously presented), the rejection of claim 32 is incorporated, and Larsen in view of Diepstraten in view of Dreyer further discloses the limitation wherein the access location allows access to determine the count without disturbing the operation of event counter (see, for example, Larsen, column 7, lines 40-52, which shows accessing the registers to read the count without disturbing the operation of the counters).

With respect to claim 34 (currently amended), the rejection of claim 33 is incorporated, and the limitations recited in the claim are analogous to those of claim 3 (see the rejection of claim 3 above).

With respect to claim 35 (currently amended), the rejection of claim 34 is incorporated, and the limitations recited in the claim are analogous to those of claim 4 (see the rejection of claim 4 above).

With respect to claim 36 (previously presented), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 7 (see the rejection of claim 7 above).

With respect to claim 37 (previously presented), the rejection of claim 36 is incorporated, and the limitations recited in the claim are analogous to those of claim 8 (see the rejection of claim 8 above).

With respect to claim 38 (currently amended), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 9 (see the rejection of claim 9 above).

With respect to claim 39 (previously presented), the rejection of claim 32 is incorporated, and the limitations recited in the claim are analogous to those of claim 30 (see the rejection of claim 30 above).

With respect to claim 40 (currently amended), Larsen discloses a machine-readable medium having stored thereon data representing sets of instructions (see, for example, column 3, lines 11-19, which shows a machine-readable medium having instructions stored thereon), the sets of instructions which, when executed by a machine (see, for example, column 4, lines 25-28, which shows executing the instructions), cause the machine to:

(a) execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event (see, for example, processor 10 in FIG. 1, and column 3, lines 39-55, which shows that the multithreaded processor simultaneously executes at least two threads, i.e. a plurality of threads, each comprising a group of instructions, and see, for example, column 6, lines 58-61, which shows that the threads result in events);

(b) instruct a first multiplexer, based on a first set of signals from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor (see, for example, control registers 80 and multiplexer 82 in FIG. 2, and column 5, lines 9-17, which shows instructing the multiplexer to select events based on the control registers, and see, for example, blocks 176, 184 and 192 in FIG. 4, and column 5, lines 41-43, which shows selecting a group or class of events from the event signals of the processor);

Although Larsen discloses selecting an event that is not masked based on the control registers (see, for example, column 5, lines 9-17), Larsen does not expressly disclose:

(c) instruct a second multiplexer, based on a second set of signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked.

However, Diepstraten discloses an event masker for masking events based on control signals from a control register, to yield subclasses of the events that are not masked (see, for example, event mask register 90 in FIG. 3, and column 4, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the machine-readable medium of Larsen with the event masking features of Diepstraten, such that the machine is caused to instruct a second multiplexer, based on a second set of control signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked. One of ordinary skill in the art would have been motivated to reduce the number of events that are to be processed (see, for example, Diepstraten, column 4, lines 42-50).

Although Diepstraten does not expressly disclose that the event masker is a multiplexer, Larson already suggests implementing such event selection as one or more multiplexers (see, for example, column 5, lines 30-36).

Larson in view of Diepstraten further discloses:

(d) qualify the event, by a logic circuit, based on a thread ID, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred (see, for example, Larsen, FIG. 3, and column 6, lines 10-23, which shows a logic circuit, and see, for example, Larsen, blocks 178 and 186 in FIG. 4, and column 6, line 54 to column 7, line 3, which shows qualifying the event based on the identity of the thread to which the event corresponds, i.e. the thread ID of the source thread of the plurality of threads where the event occurred, such as "thread 0" or "thread 1").

Although Larsen discloses qualifying the event based on a thread ID, Larsen does not expressly disclose qualifying the event based on a thread CPL.

However, Dreyer discloses a logic circuit for qualifying an event based on a thread current privilege level (CPL) (see, for example, logic block 23, control and event select register 17 and MUX 22 in FIG. 1, and column 4, lines 39-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the machine-readable medium of Larsen and Diepstraten with the thread CPL features of Dreyer, such that the machine is caused to qualify the event, by a logic circuit, based on a thread ID and a thread CPL. One of ordinary skill in the art would have been motivated to differentiate and qualify events based on supervisor and application levels of operation (see, for example, Dreyer, column 4, line 60 to column 5, line 3).

Larsen in view of Diepstraten in view of Dreyer further discloses:

(e) count the event qualified by the logic circuit using an event counter (see, for example, Larsen, performance monitor counters 84 in FIG. 2, and column 4, lines 50-57, which shows that the counters record or count the qualified events); and

(f) access the event counter to determine a current count of the event (see, for example, Larsen, integer registers 38 in FIG. 1, and column 4, lines 57-61, which shows outputting the counter values to the integer registers, i.e. the access locations, and column 7, lines 40-52, which shows accessing the registers to determine a current count of the event).

With respect to claim 41 (currently amended), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 20 (see the rejection of claim 20 above).

With respect to claim 42 (currently amended), the rejection of claim 41 is incorporated, and the limitations recited in the claim are analogous to those of claim 21 (see the rejection of claim 21 above).

With respect to claim 43 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 27 (see the rejection of claim 27 above).

With respect to claim 44 (previously presented), the rejection of claim 40 is incorporated, and the limitations recited in the claim are analogous to those of claim 28 (see the rejection of claim 28 above).

With respect to claim 45 (previously presented), the rejection of claim 41 is incorporated, and the limitations recited in the claim are analogous to those of claim 29 (see the rejection of claim 29 above).

* * *

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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